REMARKS/ARGUMENTS

Claims 4, 7-9, 13 and 16-26 are pending in the application. Claims 4, 13, 16, 20 and 24 are amended herein.

Claim Rejection under 35 USC 102(b)

Claims 4, 7, 8, 13, 16, 17, 20, 21, 24 and 25 are rejected as being anticipated by Maturi et al ("Maturi"). Maturi teaches that the host computer (host microcontroller 18) is integral to the synchronization system and is directly involved in the synchronization of the system time clock and the values provided by PCR timestamps in the MPEG bitsream. As the Examiner states in response to Applicant's previous arguments, "Furthermore, although Maturi shows a separate microcontroller and decoder system, the entire system (10) can be viewed as a computer. The entire system is the host computer which receives a stream through the receiving circuit (22)" For example, Maturi (e.g., col.8, lines 6-30) teaches that pre-parser 22 (considered by the Examiner to be equivalent to Applicant's receiver circuit) generates a first interrupt to the host microcontroller 18 and, in response, host microcontroller 18 reads system time counter 38 to obtain an initial system clock time ("SCR0"). When the PCR is parsed from the transport layer, pre-parser 22 extracts this value ("SCR1"), which is compared to SCR0 to obtain the error between the actual and requested values of the system clock time. After decoding the PES header, microcontroller 18 reads the value of the counter 38 (SCR2") and causes a new value to be set into counter 38 equal to SCR2+(SCR1-SCR0), thereby synchronizing counter 38 by compensating for the time required to decode the header.

In contrast to Maturi, the present invention maintains synchronization between the receiver circuit and the transmitter without utilizing the host computer. As explained at page 5, lines 22-23 of the present application, this synchronization is instead accomplished completely within the receiver circuit, e.g. using firmware in a transport controller. The present invention is particularly useful in applications where a direct memory access ("DMA") engine (element 119 in Fig. 1) is used to transfer elementary streams from the receiver circuit since with DMA data is transferred without requiring CPU intervention. Once the receiver circuit and transmitter are synchronized without using the host computer, a system timestamp for an application system

coupled with the decoder circuit (but not with the receiver circuit) is captured with the decoder circuit (which is part of host computer 106, e.g. as shown in Fig. 1).

In order to more particularly point out the above-described aspect of the present invention, independent claims 4, 13, 20 and 24 have been amended to specify that the receiver circuit maintains synchronization between the receiver circuit and the transmitter without utilizing the host computer. As explained above, Maturi does not anticipate or suggest this element of the present invention and therefore the amended claims patentably distinguish over Maturi. Rejected claims 7, 8, 16, 17, 21 and 25, dependent on the amended claims, also contain this element and are similarly distinguished over Maturi. Accordingly, withdrawal of the rejection and allowance of the amended claims are respectfully requested.

Claim Rejection under 35 USC 103(a)

Claims 9, 18, 22, and 26 are rejected as being obvious over Maturi. Claims 19 and 23 are rejected as being obvious over Maturi in further view of Dokic US 5699392. Each of these claims are dependent on one of the amended independent claims discussed above. Therefore, these claims incorporate the added limitation that the receiver circuit maintains synchronization between the receiver circuit and the transmitter without utilizing the host computer. As discussed, Maturi and Dokic, alone or in combination, neither teaches nor suggests this limitation. Accordingly, it is respectfully submitted that the amended claims avoid the rejection and are in condition for allowance.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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